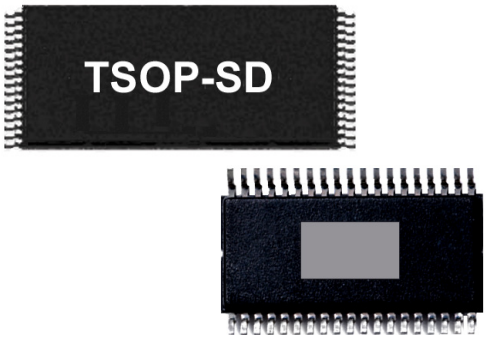
TSOP

Thin Small Outline Pack

Highlights

- Body Sizes: 12 x 20mm (48 lead); 14 x 20mm (56 lead)
- Body Thickness: 1.0mm
- Lead Pitch: 0.50mm
- Stacked Die: available between 2 to 4 die
- Stacking Options: same size die, staggered, staircase, pyramid
- LF Matrix: LD (196 x 40mm, 2 x 8 units) and HD (250 x 70mm, 4 x 10 units)



Features

- Two body sizes available in TSOP type 1 version
- Lead counts: 48 and 56
- Lead pitch: 0.50mm
- Wide range of open tool die pad sizes available; custom size available
- Moisture sensitivity: JEDEC Level 3
- JEDEC standard compliant
- Lead-free (Pb free) and green material sets available
- Copper and alloy 42 leadframes available
- Die stacking available up to 4 die

Applications

- Memory
- RF / Wireless
- Logic and Linear
- ASIC / Analog
- Processor / µController
- PC Chipset
- End applications including portable electronics, memory modules and networking equipment

Description

The Thin Small Outline Package (TSOP) is a very low-profile package with tight tight lead spacing. TSOP is available in a thermally enhanced version (TSOP-ep), as well as a stacked die version (TSOP-SD). Die stacking is available from 2 to 4 die, with bonding pads on two sides of the die or single-sided bonding pads.

TSOP delivers optimum electrical and thermal performance. Our state of the art assembly facility and proven materials assure high yield manufacturing and long term reliability.

Specifications

Single Die Thickness	10-12mils)
Stacked Die Thickness	75µm (3mils) minimum
Gold Wire	0.8mils diameter, 99.99% Au
Lead Finish	Matte Tin
Marking	Laser
Packing Options	JEDEC tray

Reliability

Moisture Sensitivity Level	JEDEC Level 3
Temperature Cycling	-65°C/150°C, 1000 cycles
Temp/Humidity Test	85°C/85%, RH, 1000 hrs
Pressure Cooker Test	121°C, 100% RH, 2 atm, 168 hrs

Thermal Performance θja (°C/W)

Package	Body Size (mm)	Die Size (mils)	Thermal Performance θja (C/W)
48L TSOP	12 x 20	150 x 150	60°C/W
48L TSOP	12 x 20	100 x 100	75°C/W

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-5) under natural convection as defined in JESD51-2.

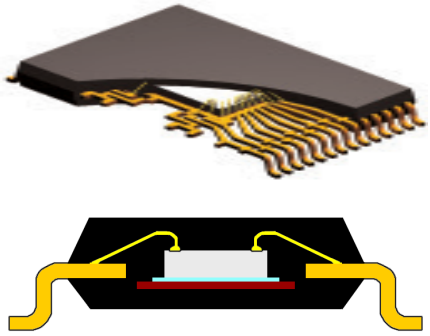
Electrical Performance

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

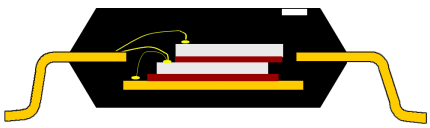
Conductor Component	Body Size (mm)	Lead/Wire (mm)	Resistance (m0hm)	Inductance (nH)	Mutal Inductance (nH)	Capacitance (pF)	Capacitance Mutual (pF)
Lead	12 x 20	6.56 - 7.60	38.0 - 44.0	3.49 - 4.17		0.69 - 0.87	
Wire		1.90	114	1.58		0.08	
Totals			152 - 158	5.07 - 5.75	2.32 - 2.62	0.77 - 0.95	0.36 - 0.39

Cross Sections

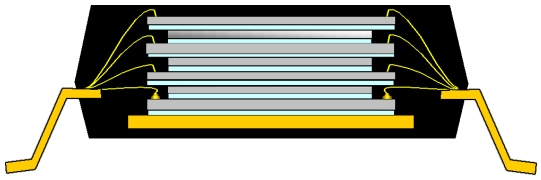
TSOP



TSOP-SD2 (2+0) staircase



TSOP-SD4 (4+3) staircase



Package Configurations

Package	Body Size	Body Thickness	Lead Count
TSOP	12 x 20mm	1.0mm	48
	14 x 20mm	1.0mm	56

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