

TQFP

Thin Profile Quad Flat Pack

Highlights

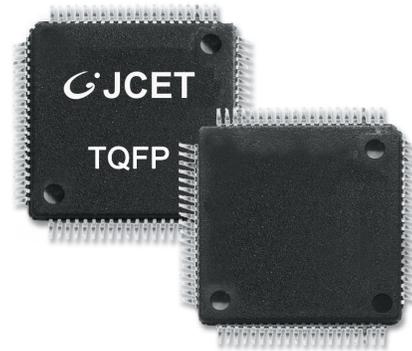
- 10 x 10mm to 16 x 16mm
- 44 to 144 lead count
- Lead pitch range from 0.50mm to 0.40mm

Features

- Body Sizes: 10 x 10mm to 16 x 16mm
- Package Height: 1.0mm
- Lead Counts: 44L to 144L
- Lead Pitch: 0.50mm to 0.40mm
- Available in gold or copper wirebond versions
- Limited number of open tool leadframe and die pad sizes available
- JEDEC standard compliant
- Lead-free, Green and Low Alpha materials sets available

Applications

- ASIC
- DSP
- Gate Array
- Logic IC
- Microprocessors
- Microcontrollers
- Multimedia
- PC Chipsets



Description

The Thin Profile Quad Flat Pack (TQFP) belongs to our QFP offering. At 1.0mm body thickness, the TQFP is the thinnest package in the QFP family. This thin package is made possible by a well controlled low loop wire bonding process and package warpage control during the molding process.

We also offer the TQFP in an Exposed Pad configuration (TQFP-ep). This is a thermally enhanced version of the TQFP package. Thermal enhancement is achieved by means of an exposed die pad, which can be soldered to a mother PC board for effective heat removal and grounding, if needed. This enhanced thermal package is made possible by a deep downset die pad leadframe design.

TQFP is suitable for mainstream cost sensitive applications where thickness and weight are premium.



Specifications

Die Thickness	230-280μm (9-11mils) range preferred
Wire	
Gold:	18-30μm (0.7-1.2mils) diameter
Copper:	18-30μm (0.7-1.2mils) diameter
Lead Finish	Matte Tin
Marking	Laser
Packing Options	Tape & reel, tube, JEDEC tray

Reliability

Moisture Sensitivity Level	JEDEC Level 3
Temperature Cycling	-65°C/150°C, 1000 cycles
High Temperature Storage	150°C, 500 hrs
Pressure Cooker Test	121°C, 100% RH, 2 atm, 168 hrs
Liquid Therapy Shock (opt)	-55°C/125°C, 1000 cycles

TQFP Thermal Performance θ_{ja} (°C/W)

Package Size	Body Size (mm)	Pad Size (mm)	Die Size (mm)	Thermal Performance θ_{ja} (C/W)
100L	14 x 14 x 1.0	9.0 x 9.0	7.8 x 7.8	38.6

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-7) under natural convection as defined in JESD51-2.

TQFP-ep Thermal Performance θ_{ja} (°C/W)

Package Size	Body Size (mm)	Pad Size (mm)	Die Size (mm)	PCB Vias	Thermal Performance θ_{ja} (C/W)
80L	12 x 12 x 1.0	7.2 x 7.2	6.0 x 6.0	36	23.0

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-7) under natural convection as defined in JESD51-2. Based on TQFP-ep simulations.

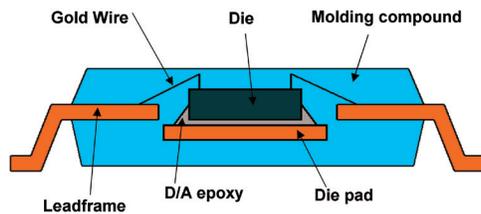
Electrical Performance

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

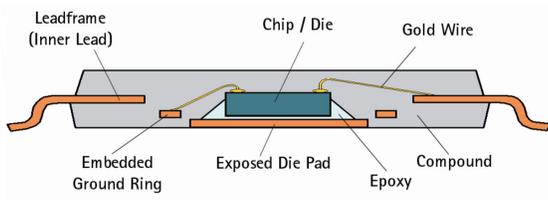
Conductor Component	Length (mm)	Resistance (mOhms)	Inductance (nH)	Mutal Inductance (nH)	Capacitance (pF)	Capacitance Mutual (pF)
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Lead (14 x 14mm, 128L)	3.0 - 4.5	24.0 - 36.0	1.96 - 2.92	1.08 - 1.61	0.45 - 0.67	0.20 - 0.30
Total (14 x 14mm, 128L)		144.0 - 156.0	3.61 - 4.57	1.53 - 2.46	0.55 - 0.77	0.21 - .032

Cross Sections

TQFP



TQFP-ep



Package Configurations

Package	Size (mm)	Lead Count
TQFP	10 x 10	44
	12 x 12	80
	14 x 14	128
	16 x 16	144
TQFP-ep	10 x 10	44
	12 x 12	80
	14 x 14	128
	16 x 16	144